FUNCTIONS OF 3.5-DIGIT WATCH CIRCUIT FOR DUPLEXED LCD

The DL9109 is low threshold voltage, CMOS integrated circuit which provides all signals to drive a duplexed 3.5-digit liquid crystal display with colon.32768Hz frequency from a crystal controlled oscillator is divided to provide second, minute, hour, date and month information. Phase controlled segment outputs and two-phase controlled back plane outputs are provide for direct drive of the duplexed LCD. The DL9109 contains an analog-digital oscillator frequency adjusting circuit. The frequency of the oscillator is divided to provide a 512Hz output pulse used as signal for the voltage doubler.

FUNCTIONS

- 5 functions: month. Date. Hour. Minute and second.
- Selective alternation of time-date display mode.
- One-touch correction of time error within 30 seconds.
- 4-year calendar.
- 2-switch operating.
- LCD test (D key and S key press simultaneously).
- Animation icon.

FEATURES

- Singe-chip CMOS construction;
- Drives 3.5-digit duplexed LCD;
- Colon display;
- 32,768HZ crystal controlled operation;
- Single 1.5V battery operation;
- On-chip capacitive voltage doubler;
- Debounce circuitry on switch inputs;
- Protection against static discharge;
- Built-in crystal oscillator network input and output capacitor.

Absolute maximum ratings (Ta=25℃)

Characteristic	Symbol	Value	Unit
Supply Voltage (V_{DD}-V_{SS})	V_{GG}	0.3~+2.0	V
Supply Voltage (V_{DD}-V_{EE})	V_{DE}	0.3~+4.6	V
Operating Temperature	T_{OPR}	0~+65	℃

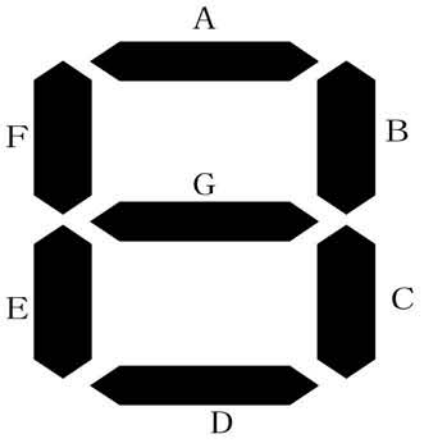
ELECTRICAL CHARACTERISTICS

(Ta=25℃, VDD=1.5V, VSS=0V; Unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating voltage	VDD		1.2	1.5	1.8	V
Doubler Output voltage	VEE		-1.2	-1.5	-1.8	V
Supply current	IDD	Without load		3	5	μA
Input low voltage	VIL		VSS		VSS+0.3	V
Input High voltage	VIH		VDD-0.3		VDD	V
Switch Activation Current	ISW	S=VDD or D= VDD		1.0	10	μA
Oscillator start Voltage	VOSC	Within 3 sec			1.25	V
Oscillator Stop Voltage	VOSP				0.95	V
Osc. Input/Output Capacitor	CI/CO			18/18		pF
Oscillator frequency	FOSC	CI=20pF, CO=20pF		32768		Hz
DC-DC Conversions Freq	VCON	C=0.1μf		512		Hz
LCD Frequency	FD			42.7		Hz

LCD FORMAT

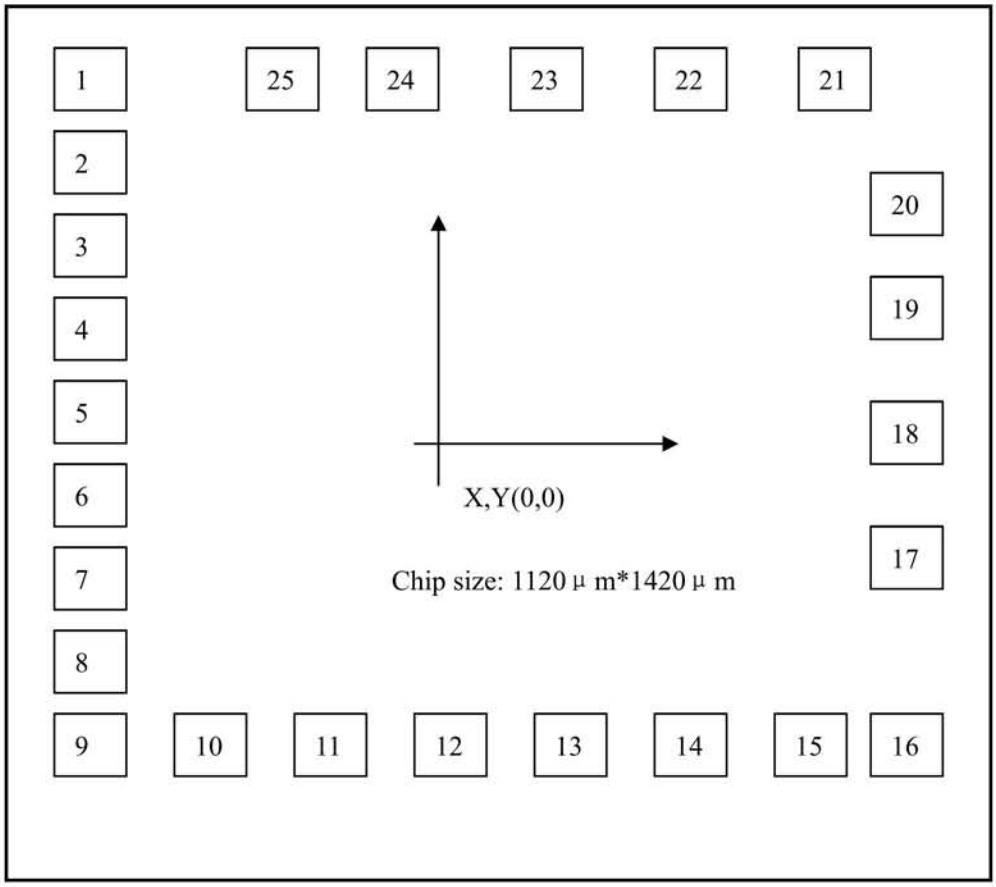
SEG	COM1	COM2	COM3		COM1	COM2	COM3
D2BC1M1	D2	BC1	M1	G3AD3M7	G3	AD3	M7
E2F2M2	E2	F2	M2	C3B3M8	C3	B3	M8
G2A2M3	G2	A2	M3	E4F4	E4	F4	
C2B2M4	C2	B2	M4	G4A4	G4	A4	
D4COLM5	D4	COL	M5	C4B4	C4	B4	
E3F3M6	E3	F3	M6				



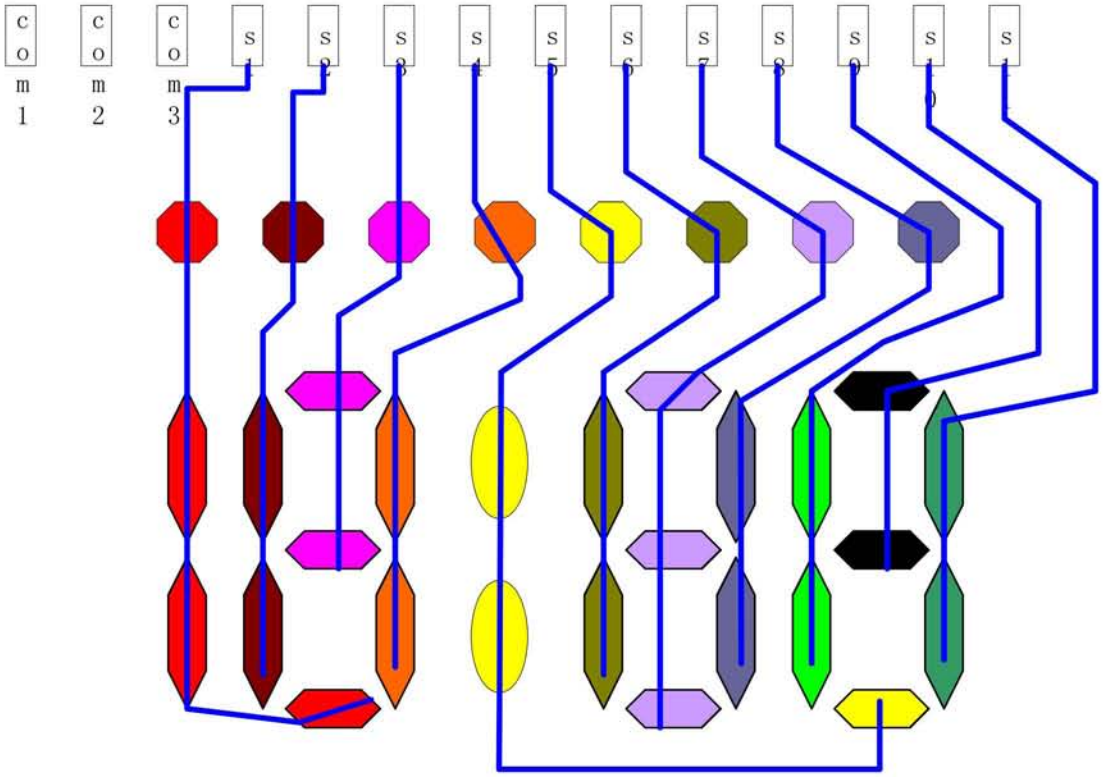
PIN DESCRIPTION

Pad NO	Symbol	Description	Pad NO	Symbol	Description
1	VDD	Battery positive	14	E4F4	Segment Output
2	T1	Test Pin 1	15	G4A4	Segment Output
3	COM1	Common	16	C4B4	Segment Output
4	COM2	Common	17	VEE	Doubled voltage
5	COM3	Common	18	T2	Test Pin 2
6	D2BC1M1	Segment Output	19	S	S key input
7	E2F2M2	Segment Output	20	D	D key input
8	G2A2M3	Segment Output	21	CAP2	Voltage Doubler
9	C2B2M4	Segment Output	22	CAP1	Voltage Doubler
10	D4COLM5	Segment Output	23	VSS	Battery negative
11	E3F3M6	Segment Output	24	OSCI	Oscillator output (with internal capacitor)
12	G3AD3M7	Segment Output	25	OSCO	Oscillator output (with internal capacitor)
13	C3B3M8	Segment Output			

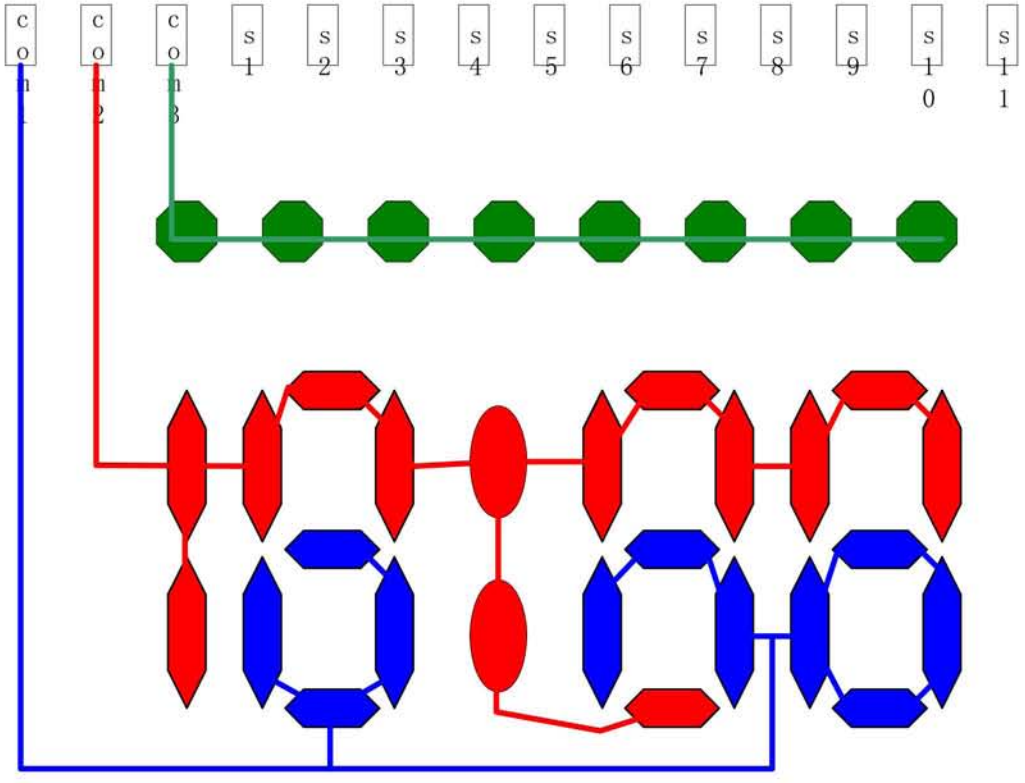
PAD DIAGRAM



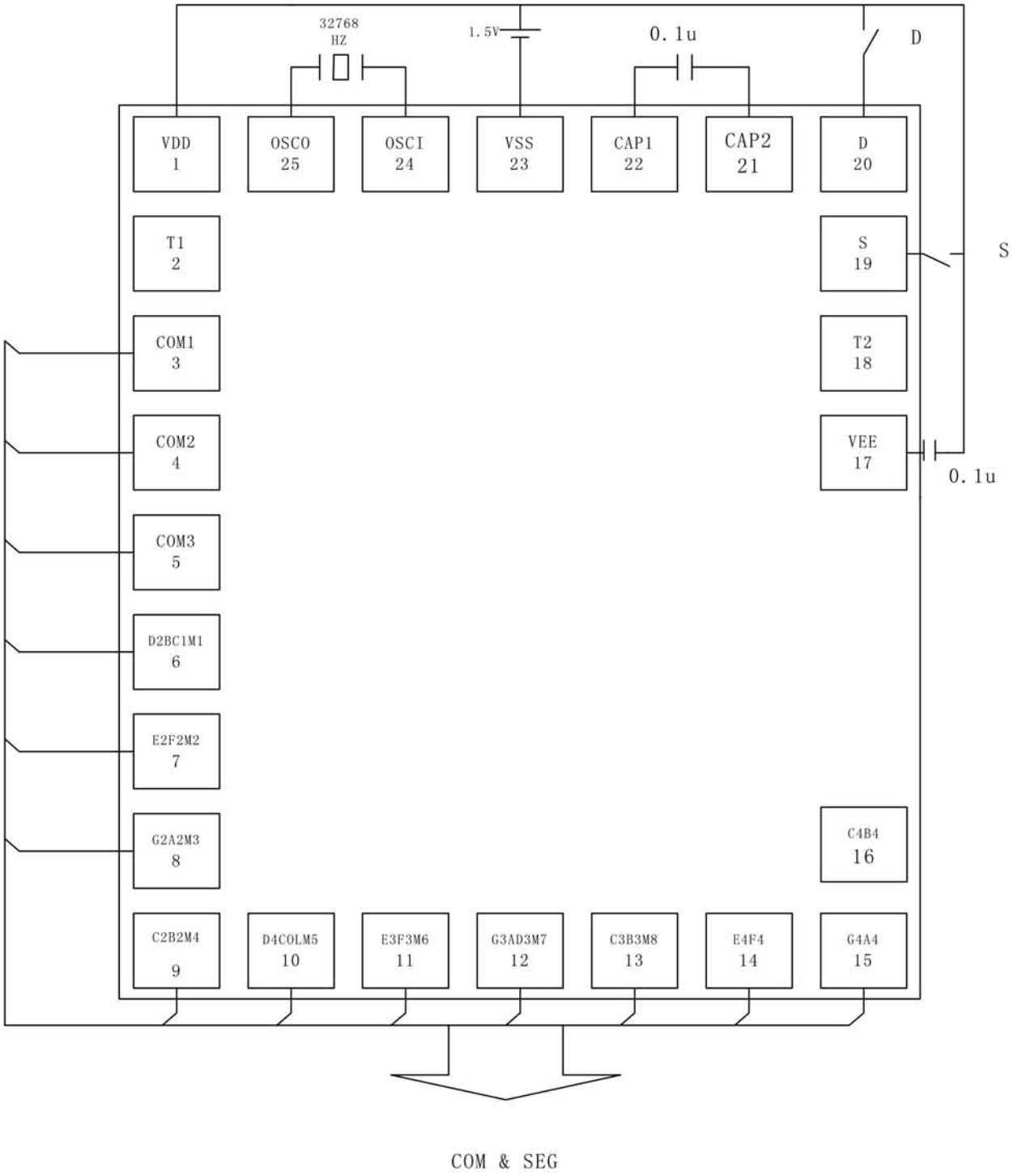
SEGMENT



COMMON



Typical Application Circuit



Note:

1. The capacitor between the VDD and VEE is optional. The customer should determine to us and optimize it according the application. （Typical value is 0.1uF）
2. Substrate is connected to VDD.